2. (Original) A semiconductor device according to claim 1, wherein the micronized pattern is a line-and-space pattern.

3. (Amended) A semiconductor device according to claim 2, wherein each of lines ~~of~~ constituting the line-and-space pattern are divided ~~by a required length~~ into a plurality of segments.

4. (Amended) A semiconductor device according to claim 3, wherein positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

Claims 5-8 (canceled)

Claims 9-12 (canceled previously)

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13. (New) A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized line-and-space pattern, and

each of lines constituting the line-and-space pattern being divided into a plurality of segments.

14. (New) A semiconductor device according to claim 13, wherein

positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

15. (New) A semiconductor device according to claim 13, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

16. (New) A semiconductor device according to claim 14, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.